IN THE CLAIMS

Following are the claims as amended herein and as are currently pending for consideration:

1-3. (Canceled)

4. (Currently Amended) A computer software product including one or more recordable media having executable instructions stored thereon which, when executed by a processing device, causes the processing device to perform, at least in part, a formal verification of a circuit or other finite-state system, said executable instructions causing the processing device to:

   initialize a symbolic simulation relation for an assertion graph on a first symbolic lattice domain, wherein the assertion graph on the first symbolic lattice domain is configurable to express a justification property to verify by computing the symbolic simulation relation.

5. (Original) The computer software product recited in Claim 4 which, when executed by a processing device, further causes the processing device to:

   compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain; and

   check the symbolic simulation relation to verify a plurality of properties expressed by a plurality of assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

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6-7. (Canceled)

8. (Currently Amended) A computer software product including one or more recordable media having executable instructions stored thereon which, when executed by a processing device, causes the processing device to perform, at least in part, a formal verification of a circuit or other finite-state system, said executable instructions causing the processing device to:

    initialize a symbolic simulation relation for an assertion graph on a first symbolic lattice domain; and

    compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain to verify the assertion graph according to a normal satisfiability criteria.

9-13. (Canceled)

14. (Currently Amended) A computer implemented method for performing, at least in part, a formal verification of a circuit or other finite-state system, said method comprising:

    initializing a symbolic simulation relation for an assertion graph on a first symbolic lattice domain, wherein the assertion graph on the first symbolic lattice domain is configurable configured to express a justification property to verify through computing the symbolic simulation relation.

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15. (Original) The method recited in Claim 14 further comprising:

computing the symbolic simulation relation for the assertion graph on the first symbolic lattice domain; and

checking the symbolic simulation relation to verify a plurality of properties expressed by a plurality of corresponding assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

16. (Currently Amended) A <u>computer implemented</u> method <u>for performing, at least in part, a formal verification of a circuit or other finite-state system, said method</u> comprising:

specifying a justification property with an assertion graph.

17. (Original) The method recited in Claim 16 wherein the assertion graph is on a first symbolic lattice domain; and the justification property is expressed by one of a plurality of instances of the assertion graph, at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

18. (Original) The method recited in Claim 17 further comprising:

computing a symbolic simulation relation for the assertion graph on the first symbolic lattice domain; and

checking the symbolic simulation relation with a symbolic consequence labeling for the assertion graph on the first symbolic lattice domain according to a normal satisfiability criteria.

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19-27. (Canceled)

28. (Currently Amended) A <u>computer implemented</u> verification system <u>for performing,</u>

<u>at least in part, a formal verification of a circuit or other finite-state system, said</u>

<u>system</u> comprising:

means for initializing a symbolic simulation relation for an assertion graph on a

first symbolic lattice domain, wherein the assertion graph on the first symbolic lattice

domain is ~~configurable~~ <u>configured</u> to express a justification property to verify through

computing the symbolic simulation relation;

means for computing the symbolic simulation relation for the assertion graph on

the first symbolic lattice domain; and

means for checking the symbolic simulation relation to verify a plurality of

properties expressed by a plurality of corresponding assertion graph instances, having

at least one assertion graph instance on a second lattice domain different from the first

symbolic lattice domain.

29-30. (Canceled)